VLSI SIGNAL PROCESSING

PROF. MRITYUNJAY CHAKRABORTY
Department of Electrical and Electronics Engineering
IIT Kharagpur

TYPE OF COURSE : Rerun | Elective | UG/PG
COURSE DURATION : 8 weeks (21 Feb' 22 - 15 Apr' 22)
EXAM DATE : 24 Apr 2022

INTENDED AUDIENCE : Electrical Engg., Electronics and Communication Engg., Instrumentation Engg., Information technology and Computer Science students
INDUSTRIES APPLICABLE TO : ST Microelectronics Ltd, Texas Instruments, Ittiam Systems

COURSE OUTLINE :

Digital signal processing (DSP) has emerged over last two decades as the single most key component in all electronic applications, e.g., multimedia and mobile communications, video compression, digital still and network cameras, mobile phones, radar imaging, acoustic beamformers, GPS, biomedical signal processing etc. Most of these applications impose several challenges in the implementation of DSP systems, like capability to process high throughput data as demanded by the real time application, as well as requiring less power and less chip area.This course aims at providing a comprehensive coverage of some of the important techniques for designing efficient VLSI architectures for DSP. Towards this, architectural optimization at various levels will be considered. The course assumes minimal prerequisites - an undergraduate level knowledge of digital circuit design and elementary DSP operations is sufficient for one to be able to attend the course. Apart from regular students, participants from academia may thus find the course to be useful to develop similar courses at their respective institutions. Alternatively, the course may also be used as a reference by industrial professionals interested in VLSI design of signal processing and communication systems.

ABOUT INSTRUCTOR :

Prof. Mrityunjoy Chakraborty obtained Bachelor of Engg. from Jadavpur university, Calcutta, Master of Technology from IIT, Kanpur and Ph.D. from IIT, Delhi. He joined IIT, Kharagpur as a faculty member in 1994, where he currently holds the position of a professor in Electronics and Electrical Communication Engg. The teaching and research interests of Prof. Chakraborty are in Digital and Adaptive Signal Processing, VLSI Signal Processing, Linear Algebra and Compressive Sensing. In these areas, Prof. Chakraborty has supervised several graduate theses, carried out independent research and has several well cited publications. Prof. Chakraborty is currently a senior editorial board member of the IEEE Signal Processing Magazine and also of the IEEE journal of Emerging Techniques in Circuits and Systems. Earlier, he had been an Associate Editor of the IEEE Transactions on Circuits and Systems, part I (2004-2007, 2010-2012) and part II (2008-2009), apart from being an elected member (also currently the chair) of the DSP Technical Committee (TC) of the IEEE Circuits and Systems Society, a guest editor of the EURASIP JASP (special issue), track co-chair (DSP track) of ISCAS 2015 & 2016, Gabor track chair of DSP-15, and a TPC member of ISCAS (2011-2014), ICC (2007-2011) and Globecom (2008-2011). Prof. Chakraborty is a co-founder of the Asia Pacific Signal and Information Processing Association (APSIPA), is currently a member of the APSIPA BOG and also, served as the chair of the APSIPA TC on Signal and Information Processing Theory and Methods (SIPTM). He has also been the general chair and also the TPC chair of the National Conference on Communications – 2012. Prof. Chakraborty is a fellow of the National Academy of Science, India (NASI), and also of the Indian National Academy of Engineering (INAE). During 2012-2013, he was selected as a distinguished lecturer of the APSIPA.

COURSE PLAN :

Week 1**:** Graphical representation of DSP algorithms, signal flow graph (SFG), data flow graph (DFG) and dependence graph (DG), high level transformation, critical path.

Week 2: Retiming of DFG, critical path minimization by retiming, loop retiming and iteration bound
Week 3: Cutset retiming, design of pipelined DSP architectures, examples

Week 4: Parallel realization of DSP algorithms, idea of unfolding, unfolding theorem, loop unfolding
Week 5: Polyphase decomposition of transfer functions, hardware efficient parallel realization of FIR filters, 2-parallel and 3-parallel filter architectures.

Week 6: Hardware minimization by folding, folding formula, examples from biquad digital filters,

Week 7: Delay optimization by folding, lifetime analysis, forward-backward data allocation, examples from digital filters

Week 8: Pipelining digital filters, look ahead techniques, clustered and scattered look ahead, combining parallel processing with pipelining in digital filters